In the Claims:

1. (Currently Amended) A memory device comprising:

(a) a first, directly executable memory for storing boot code of a computer, said boot code including code that is executed first by said computer when said computer is powered up;

(b) a second memory; and

(c) a single connector, for operationally connecting said two memories to said computer, that includes:

(i) a first plurality of pins for supporting communication between said first memory and said computer, and

(ii) a second plurality of pins for supporting communication between said second memory and said computer,

said first and second pluralities of pins sharing at least one said pin; and

(d) a switch for alternately connecting said first memory and said second memory to said computer via said at least one shared pin.

2. (Original) The device of claim 1, wherein said operational connection is reversible.

3. (Original) The device of claim 1, wherein said operational connection is permanent.

4. (Original) The device of claim 1, wherein said first memory is a read-only memory.

5. (Original) The device of claim 1, wherein said second memory is for storing an operating system of said computer.

6. (Original) The device of claim 1, wherein said second memory is a magnetic disk memory.

7. (Original) The device of claim 1, wherein said second memory is a flash memory.

8. (Original) The device of claim 1, further comprising:

(d) a Universal Serial Bus (USB) controller for supporting communication between said second memory and said computer.

9. (Original) The device of claim 8, wherein at least one of said memories stores a read-only USB driver.

10. (Original) The device of claim 9, wherein said read-only USB driver is stored in said first memory.

11. (Canceled)

12. (Currently Amended) The device of claim **[[11]]**52, wherein said first and second pluralities of pins are separate.

13-15. (Canceled)

16. (Currently Amended) The device of claim **[[15]]**52, wherein said first protocol is a Low Pin Count (LPC) protocol.

17. (Currently Amended) The device of claim **[[15]]**52, wherein said second protocol is a Universal Serial Bus (USB) protocol.

18-24. (Canceled)

25. (Currently Amended) A computer peripheral device comprising:

(a) a first component;

(b) a second component separate from said first component;

(c) a connector, for operationally connecting said first and second components to a computer, that includes:

(i) a first plurality of pins for supporting communication between said first component and said computer, and

(ii) a second plurality of pins for supporting communication between said second component and said computer,

said first and second pluralities of pins sharing at least one said pin;

[[and]]

(d) a single Universal Serial Bus (USB) controller for supporting communication only between said first component and said computer; and

(e) a switch for alternately connecting said first component and said second component to said computer via said at least one shared pin.

26. (Original) The device of claim 25, wherein said first component is a memory.

27. (Original) The device of claim 26, wherein said memory is a magnetic disk memory.

28. (Original) The device of claim 26, wherein said memory is a flash memory.

29. (Original) The device of claim 25, wherein said second component is a directly executable memory for storing boot code.

30. (Original) The device of claim 29, wherein said connector supports a Low Pin Count (LPC) protocol for said second component.

31. (Original) The device of claim 29, wherein said directly executable memory is a read-only memory.

32. (Original) The device of claim 25, wherein said operational connection is reversible.

33. (Canceled):

34. (Currently Amended) The device of claim **[[33]]**53, wherein said first and second pluralities of pins are separate.

35-37. (Canceled)

38. (Currently Amended) The device of claim **[[33]]**25, wherein said second plurality of pins includes separate respective pins for address signals and data signals.

39. (Currently Amended) A method of operating a computer, comprising the steps of:

(a) providing at least one memory device including:

(i) a respective first, directly executable memory, and

(ii) a respective second memory;

(b) for each said at least one memory device, storing boot code of the computer in said respective first memory, said boot code including code that is executed first by the computer when the computer is powered up;

(c) operationally connecting one of said at least one memory device to the computer; **[[and]]**

(d) executing said boot code that is stored in said respective first memory of said one memory device, by the computer and

(e) for each said at least one memory device, storing an operating system of the computer in said respective second memory;

wherein said executing of said boot code includes copying said operating system from said respective second memory of said one memory device to the computer;

wherein, for each said at least one memory device, said boot code includes driver code for said respective second memory;

and wherein said copying of said operating system from said respective second memory of said one memory device to the computer is effected by executing at least a portion of said driver code.

40. (Original) The method of claim 39, wherein said operational connection is reversible.

41-42. (Canceled)

43. (Currently Amended) The method of claim **[[42]]**39, wherein said driver code is read-only driver code.

44. (Currently Amended) The method of claim **[[41]]**39, wherein a plurality of said memory devices are provided, each said memory device having a respective operating system of the computer stored in said second memory thereof; and wherein all said respective operating systems are different.

45. (Original) The method of claim 39, wherein all of said boot code is executed directly from said first memory.

46-51. (Canceled)

52. (New) A memory device comprising:

(a) a first, directly executable memory for storing boot code of a computer, said boot code including code that is executed first by said computer when said computer is powered up;

(b) a second memory; and

(c) a single connector, for operationally connecting said two memories to said computer, that includes:

(i) a first plurality of pins for supporting communication between said first memory and said computer, said first plurality of pins being for a first access protocol that supports direct execution of said boot code and

(ii) a second plurality of pins for supporting communication between said second memory and said computer, said second plurality of pins being for a second, serial access protocol.

53. (New) A computer peripheral device comprising:

(a) a first component;

(b) a second component separate from said first component;

(c) a connector, for operationally connecting said first and second components to a computer, that includes:

(i) a first plurality of pins for supporting communication between said first component and said computer, and

(ii) a second plurality of pins for supporting communication between said second component and said computer, said

communication between said second component and said computer multiplexing said second plurality of pins; and

(d) a single Universal Serial Bus (USB) controller for supporting communication only between said first component and said computer.

54. (New) A method of operating a computer, comprising the steps of:

(a) providing at least one memory device including:

(i) a respective first, directly executable memory, and

(ii) a respective second memory;

(b) for each said at least one memory device, storing boot code of the computer in said respective first memory, said boot code including code that is executed first by the computer when the computer is powered up;

(c) operationally connecting one of said at least one memory device to the computer; and

(d) executing said boot code that is stored in said respective first memory of said one memory device, by the computer, by steps including:

(i) executing only a portion of said boot code directly from said first memory;

(ii) copying a remainder of said boot code to a random access memory; and

(iii) executing said reminder of said boot code from said random access memory.